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ISSUE CLASSIFICATION	
Class	Subclass

FA 0 O.I.P.E. 1 AA
SCANNED SA Q.A. 1

PATENT DATE

APPLICATION NO. 09/819940	CONT/PRIOR	CLASS 348 375	SUBCLASS 240.16	ART UNIT 2613	EXAMINER Diep
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APPLICANTS

Fabrizio Rovati
Danilo Rau
Emiliano Piccinelli

TIME

Coprocessor circuit architecture, for instance for digital encoding applications

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		NOTICE OF ALLOWANCE MAILED	
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<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	REST AVAILABLE		ISSUE FEE	
	_____ (Primary Examiner)		Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		ISSUE BATCH NUMBER	
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